INPUT BUFFER CIRCUIT

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Abstract of the Disclosure

An input buffer circuit simultaneously supports a low voltage interface and a general low voltage transistor-transistor logic (LVTTL) interface and operates at high speed. In the input buffer circuit, a self bias voltage generated by a self biased differential amplification circuit is used not only for tracking a common mode input voltage in the differential amplification circuit but also for controlling the current of a current source and/or sink that controls the current used in the differential amplification circuit. Accordingly, the self bias voltage remains at a substantially uniform level. Therefore, the entire transconductance gain gm of the differential amplification circuit is substantially uniform regardless of the change in a reference voltage input to the differential amplification circuit. As a result, a low voltage interface characteristic is improved. The input buffer circuit further can further include a swing width control circuit that responds to an inverted signal generated from the output signal of the differential amplification circuit and prevents the voltage swing of the output signal from becoming excessively large. This reduces skew and thus improves the operating speed of the input buffer.